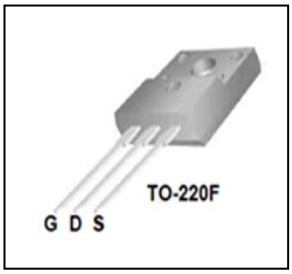
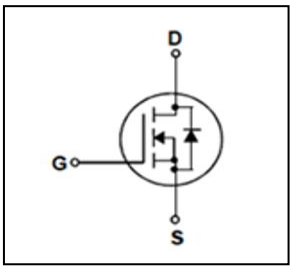
# 900V N-Channel MOSFET

**General Description**

This Power MOSFET is produced using advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.




**Features**

7A, 900V, $R_{DS}$(on)typ. = 1. 65Ω@VGS = 10 V
Low gate charge (41.5nC)
High ruggedness
Fast switching
Improved dv/dt capability

## Absolute Maximum Ratings $T_C$ = 25 ℃ unless otherwise noted

| Symbol | Parameter | | JFFM7N90C | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain – Source Voltage | | 900 | V |
| $I_D$ | Drain Current | Continuous ( $T_C$ = 25 ℃ ) | 7 | A |
| | | Continuous ( $T_C$ = 100 ℃ ) | 4* | A |
| $I_{DM}$ | Drain Current - Pulsed | ( Note 1 ) | 28 | A |
| $V_{GSS}$ | Gate – Source Voltage | | ±30 | V |
| EAS | Single Pulsed Avalanche Energy | ( Note 2 ) | 258 | mJ |
| $I_{AR}$ | Avalanche Current | ( Note 1 ) | 7 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | ( Note 1 ) | 20 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | ( Note 3 ) | 5.0 | V/ns |
| $P_D$ | Power Dissipation ( $T_C$ = 25 ℃ ) | | 48 | W |
| | -Derate above 25 ℃ | | 0.364 | W/℃ |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | | -55~150 | ℃ |
| $T_L$ | Maximum lead temperature for soldering purposes 1/8” frome case for 5 seconds | | 300 | ℃ |

*Drain current limited by maximum junction temperature.

## Thermal characteristics

| Symbol | Parameter | JFFM7N90C | Units |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 2.6 | ℃/W |
| $R_{\theta JS}$ | Thermal Resistance, Case-to-Sink Typ. | -- | ℃/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 62.5 | ℃/W |

## Electrical Characteristics $T_C$ = 25 ℃ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain – Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 uA | 900 | -- | -- | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 uA, Referenced to 25℃ | -- | 0.65 | -- | V/℃ |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 900 V, $V_{GS}$ = 0 V | -- | -- | 1 | uA |
| | | $V_{DS}$ = 720 V, Tj = 125 ℃ | -- | -- | 10 | uA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 30 V, $V_{GS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -30 V, $V_{GS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 uA | 3.0 | -- | 5.0 | V |
| $R_{DS(on)}$ | Static Drain-Source on-Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.5A | -- | 1.65 | 2.15 | Ω |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 20 V, $I_D$ = 3.5 A ( Note 4 ) | -- | 8.2 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 1540 | -- | pF |
| $C_{oss}$ | Output Capacitance | | -- | 108 | -- | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 8.19 | -- | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DS}$ = 520 V, $I_D$ = 7.0 A , $R_G$ = 25Ω , $V_{GS}$ = 10 V (Note 4,5 ) | -- | 19 | -- | ns |
| $t_r$ | Turn-On Rise Time | | -- | 15 | -- | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 80 | -- | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 22 | -- | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 630 V, $I_D$ = 7.0 A $V_{GS}$ = 10 V (Note 4,5 ) | -- | 41.5 | -- | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 8.15 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 14.95 | -- | nC |
| **Drain – Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 7 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 28 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 7.0 A | -- | 0.87 | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_S$ = 7.0 A $dI_F/dt$ = 100 A/us ( Note 4 ) | -- | 330 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 2.5 | -- | uC |

**Notes:**

1. Repetitive Rating : Pulsed width limited by maximum junction temperature
2. L = 10mH , $I_{AS}$ = 7A, $V_{DD}$ = 50V,$R_G$ = 25Ω, Starting $T_J$ = 25℃
3. $I_{SD}$ ≤ 7.0A, di/dt ≤ 200A/us, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulsed Test : Pulsed width ≤300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

## Typical Characteristics

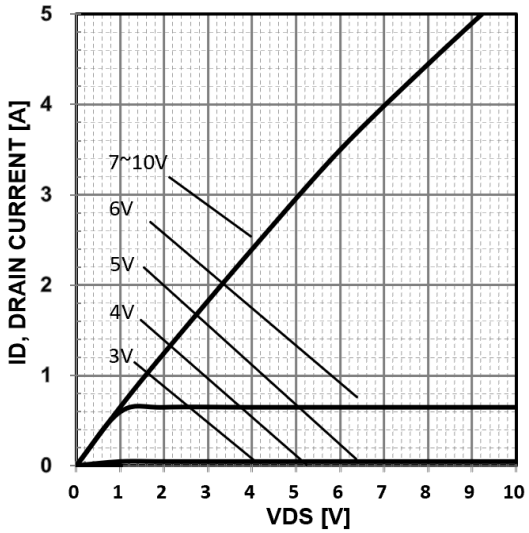



Figure 1. Typical Output Characteristics, Tc=25℃

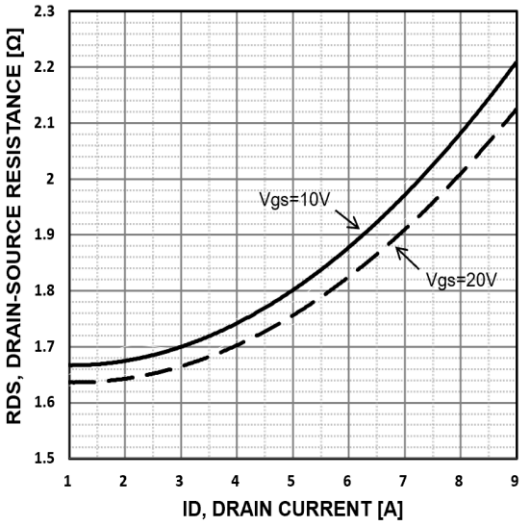



Figure 2. On-Resistance Vs.Drain Current and Gate Voltage

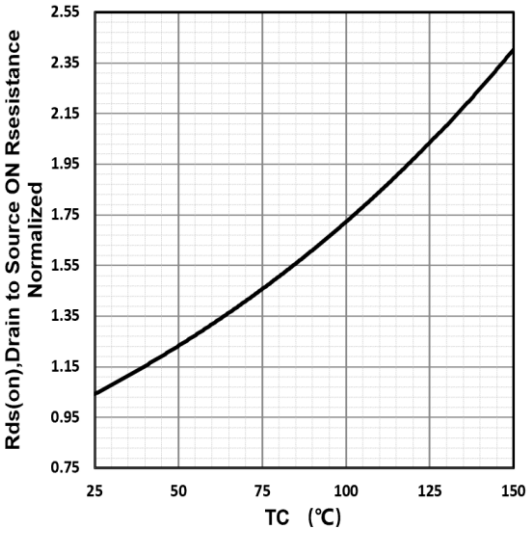



Figure 3. Normalized On-Resistance Vs.Temperature

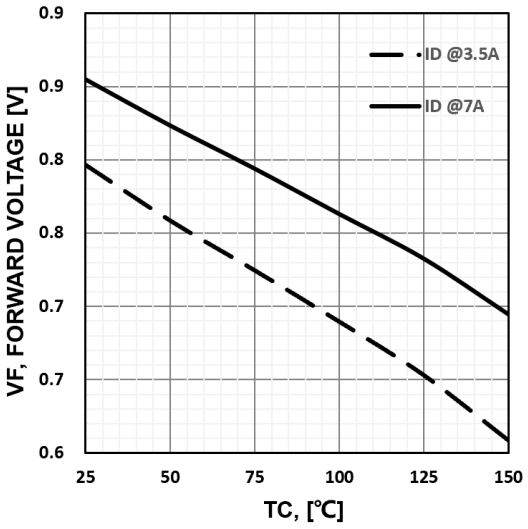



Figure 4. Forward Voltage Vs.Temperature

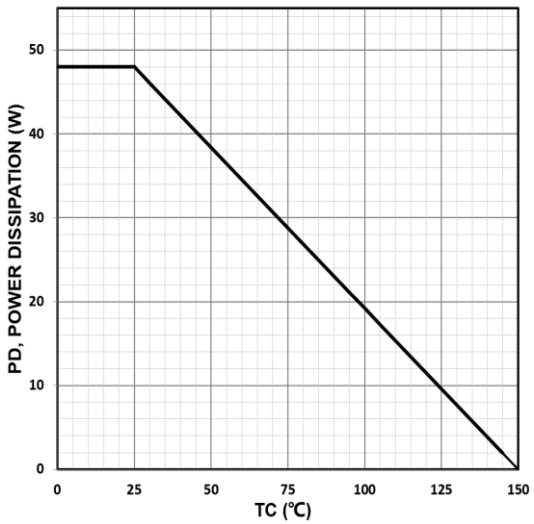



Figure 5. Power Dissipation Vs.Temperature

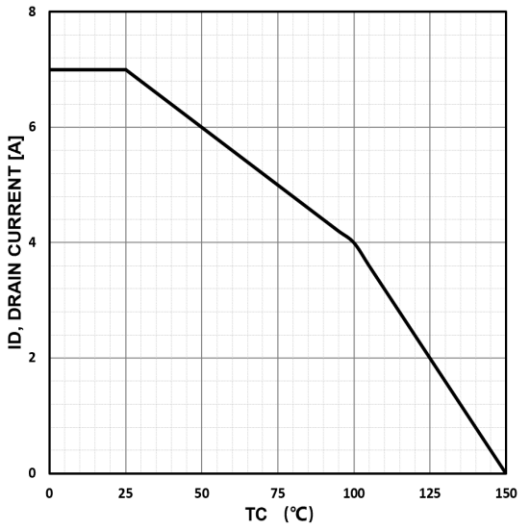



Figure 6. Drain Current Vs.Temperature

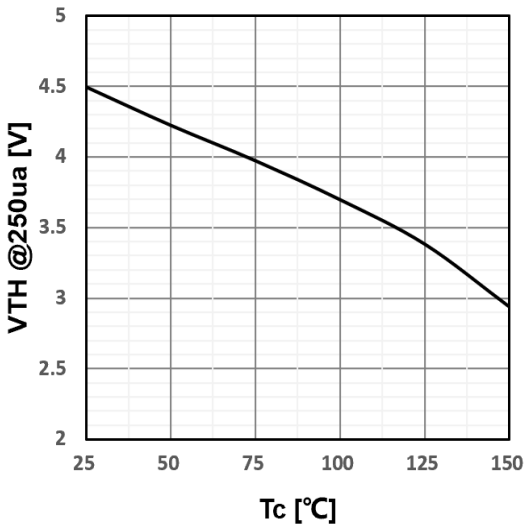



Figure 7. Vth @250ua Vs.Temperature

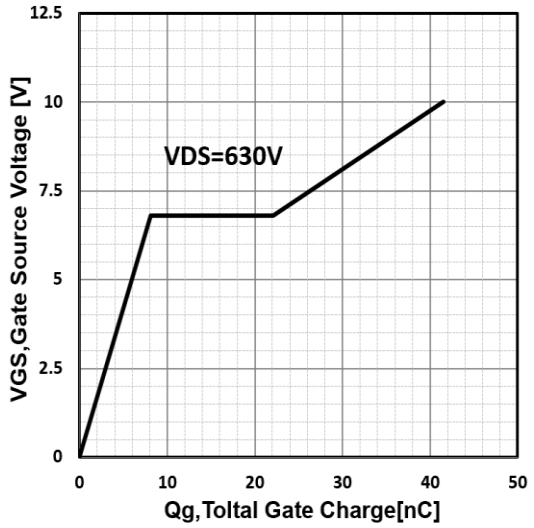



Figure 8. Gate Charge

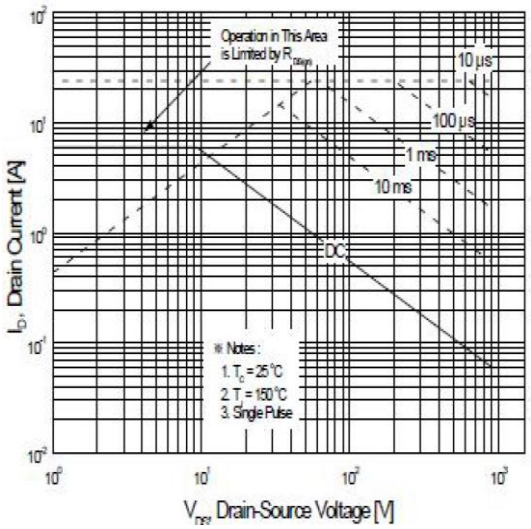
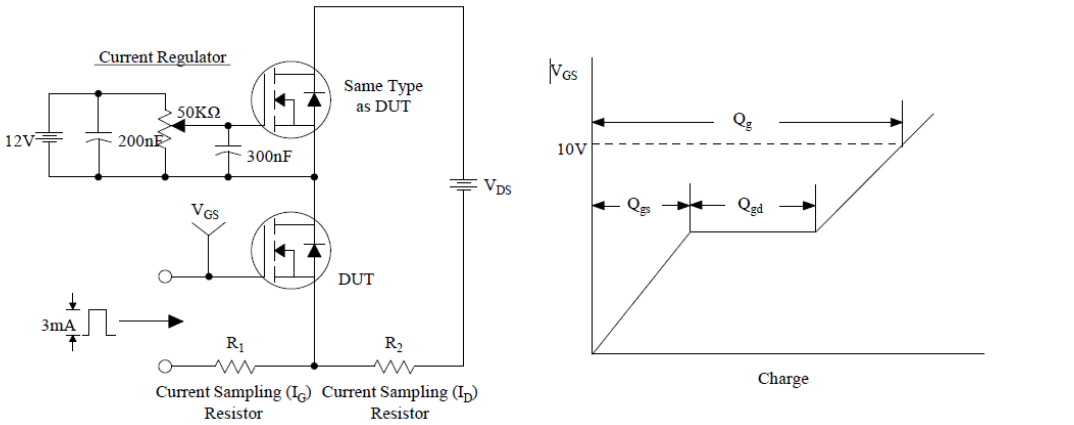
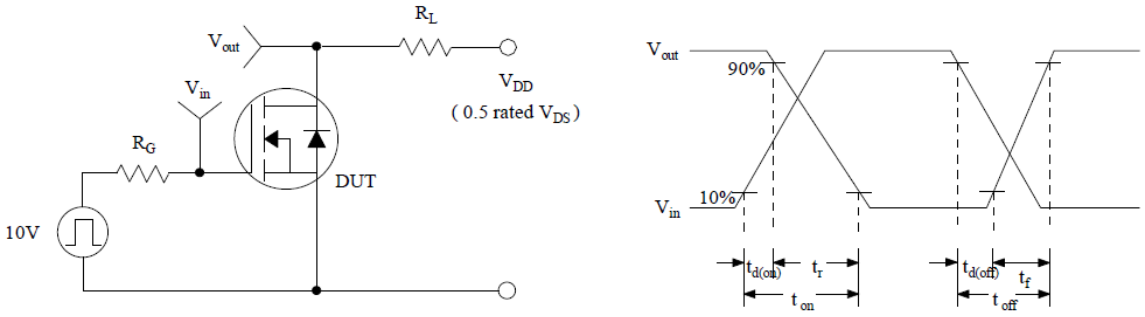


Figure 9. Maximum Safe Operating Area

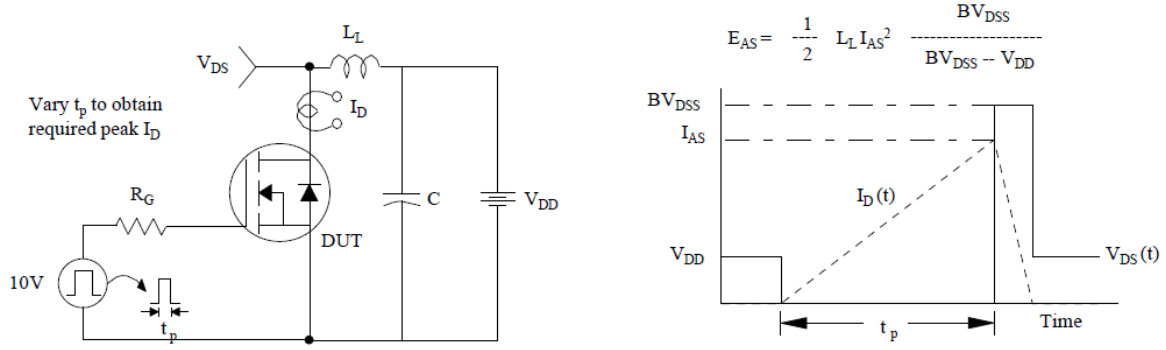
## Test Circuit & Waveform




Gate Charge Test Circuit & Waveform

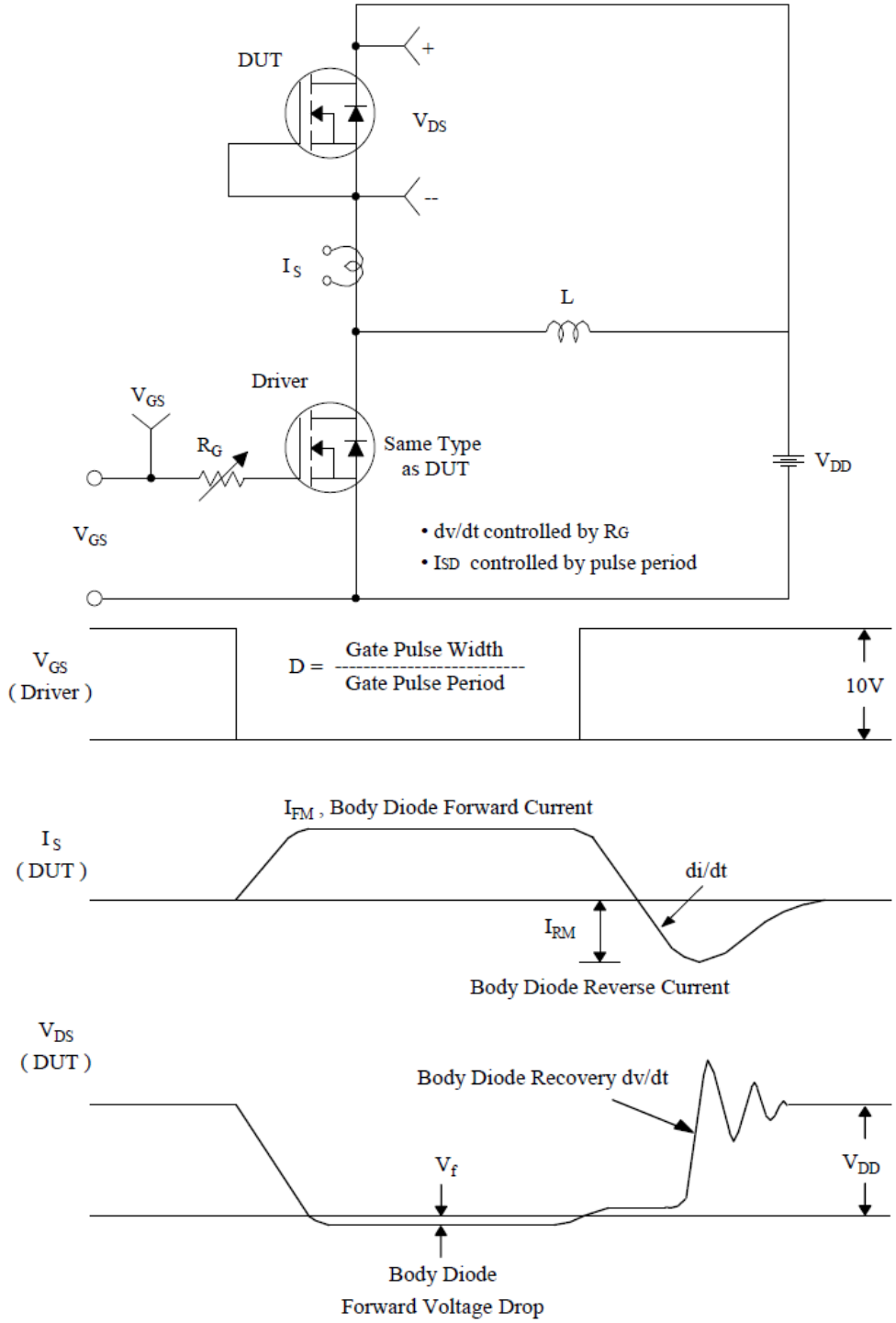



Resistive Switching Test Circuit & Waveforms



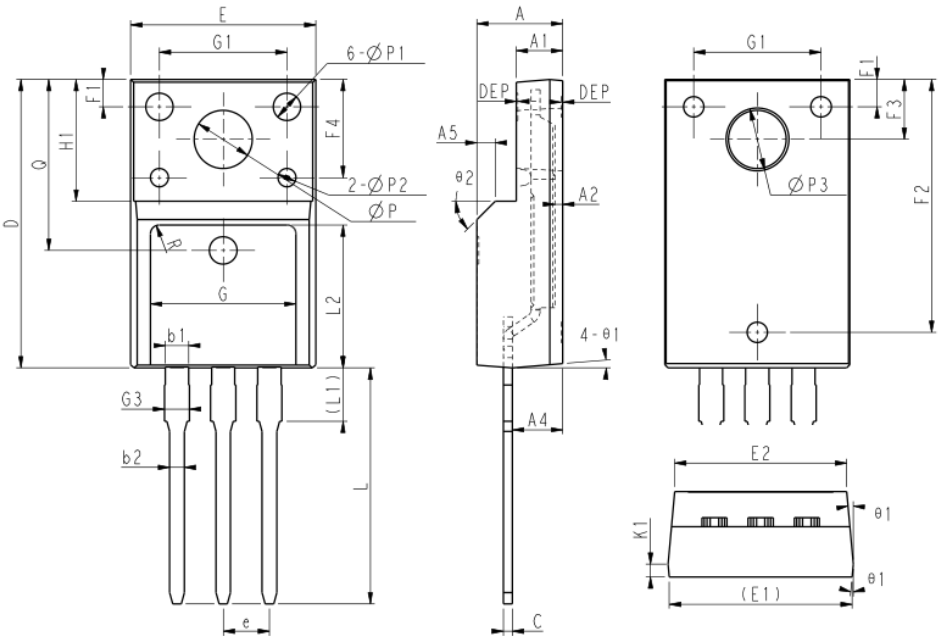

Unclamped Inductive Switching Test Circuit & Waveforms

## Test Circuit & Waveform




Peak Diode Recovery dv/dt Test Circuit & Waveforms

## TO-220F Package




COMMON DIMENSIONS

| SYMBOL | MM | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| E | 10.00 | 10.16 | 10.32 |
| E1 | 9.94 | 10.04 | 10.14 |
| E2 | 9.36 | 9.46 | 9.56 |
| A | 4.50 | 4.70 | 4.90 |
| A1 | 2.34 | 2.54 | 2.74 |
| A2 | 0.43 | - | 0.48 |
| A4 | 2.66 | 2.76 | 2.86 |
| A5 | | 1.00REF | |
| c | 0.45 | 0.50 | 0.60 |
| D | 15.67 | 15.87 | 16.07 |
| Q | | 9.40REF | |
| H1 | | 6.70REF | |
| e | | 2.54BSC | |
| ΦP | | 3.18REF | |
| L | 12.78 | 12.98 | 13.18 |
| L1 | 2.83 | 2.93 | 3.03 |
| L2 | 7.70 | 7.80 | 7.90 |
| ΦP1 | 1.40 | 1.50 | 1.60 |
| ΦP2 | 0.95 | 1.00 | 1.05 |
| ΦP3 | | 3.45REF | |
| θ1 | 3° | 5° | 7° |
| θ2 | - | 45° | - |
| DEP | 0.05 | 0.10 | 0.15 |
| F1 | 1.00 | 1.50 | 2.00 |
| F2 | 13.80 | 13.90 | 14.00 |
| F3 | 3.20 | 3.30 | 3.40 |
| F4 | 5.30 | 5.40 | 5.50 |
| G | 7.80 | 8.00 | 8.20 |
| G1 | 6.90 | 7.00 | 7.10 |
| G3 | 1.25 | 1.35 | 1.45 |
| b1 | 1.23 | 1.28 | 1.38 |
| b2 | 0.75 | 0.80 | 0.90 |
| K1 | 0.65 | 0.70 | 0.75 |
| R | | 0.50REF | |

# Disclaimers

JIAEN Semiconductor Co., Ltd reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to JIAEN's terms and conditions supplied at the time of order acknowledgement.

JIAEN Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing, reliability and quality control are used to the extent JIAEN deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

JIAEN Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using JIAEN's components. To minimize risk, customers must provide adequate design and operating safeguards.

JIAEN Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its parent rights, nor the rights of others. Reproduction of information in JIAEN's datasheets or data books sis permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. JIAEN Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of JIAEN's products with statements different from or beyond the parameters stated by JIAEN Semiconductor Co., Ltd for that product or service voids all express or implied warrantees for the associated JIAEN's product or service and is unfair and deceptive business practice. JIAEN Semiconductor Co., Ltd is not responsible or liable for any such statements.