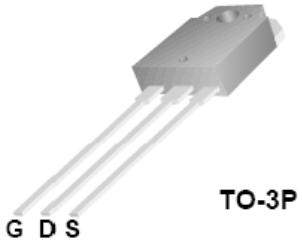
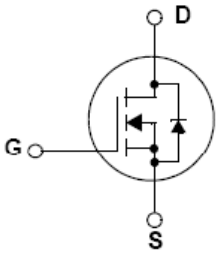
500V N-Channel MOSFET

General Description

This Power MOSFET is produced using advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.





Features

30A, 500V, R_{DS}(on)typ. = 0.17Ω@VGS = 10 V
Advanced planar process
Low gate charge minimize switching loss
Fast switching
100% avalanche tested
Improved dv/dt capability

Absolute Maximum Ratings T_C = 25 ℃ unless otherwise noted

Symbol	Parameter		JFAM30N50E	Units
V_{DSS}	Drain – Source Voltage		500	V
I_D	Drain Current	Continuous (T_C = 25 ℃)	30*	A
		Continuous (T_C = 100 ℃)	17*	A
I_{DM}	Drain Current - Pulsed (Note 1)		105	A
V_{GSS}	Gate – Source Voltage		±30	V
EAS	Single Pulsed Avalanche Energy (Note 2)		2227	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		5.0	V/ns
P_D	Power Dissipation (T_C = 25 ℃)		300	W
	-Derate above 25 ℃		2.4	W/℃
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃
T_L	Maximum lead temperature for soldering purposes 1/8” frome case for 5 seconds		300	℃

*Drain current limited by maximum junction temperature.

Thermal characteristics

Symbol	Parameter	JFAM30N50E	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.42	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	50	℃/W

Electrical Characteristics T_C = 25 ℃ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain – Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 uA	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 uA, Referenced to 25℃	--	0.5	--	V/℃
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	uA
		V_{DS} = 400 V, Tc = 125 ℃	--	--	100	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{GS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{GS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 uA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source on-Resistance	V_{GS} = 10 V, I_D = 15A	--	0.17	0.21	Ω
g_{FS}	Forward Transconductance	V_{DS} = 25 V, I_D = 15 A (Note4)	--	32	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	4050	--	pF
C_{oss}	Output Capacitance		--	445	--	pF
C_{rss}	Reverse Transfer Capacitance		--	80	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 250 V, I_D = 30.0 A , R_G = 10Ω , V_{GS} = 10 V (Note 4,5)	--	32	--	ns
t_r	Turn-On Rise Time		--	105	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	95.5	--	ns
t_f	Turn-Off Fall Time		--	67.5	--	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 30.0 A V_{GS} = 10 V (Note 4,5)	--	80	--	nC
Q_{gs}	Gate-Source Charge		--	22	--	nC
Q_{gd}	Gate-Drain Charge		--	23	--	nC
Drain – Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	30	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	105	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 30.0 A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 30.0 A dI_F/dt = 100 A/us (Note 4)	--	530	--	ns
Q_{rr}	Reverse Recovery Charge		--	4.5	--	uC

Notes:

1. Repetitive Rating : Pulsed width limited by maximum junction temperature
2. L = 4.5mH , I_{AS} = 30A, V_{DD} = 50V,R_G = 25Ω, Starting T_J = 25℃
3. I_{SD} ≤ 20.0A, di/dt ≤ 200A/us, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulsed Test : Pulsed width ≤300us, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

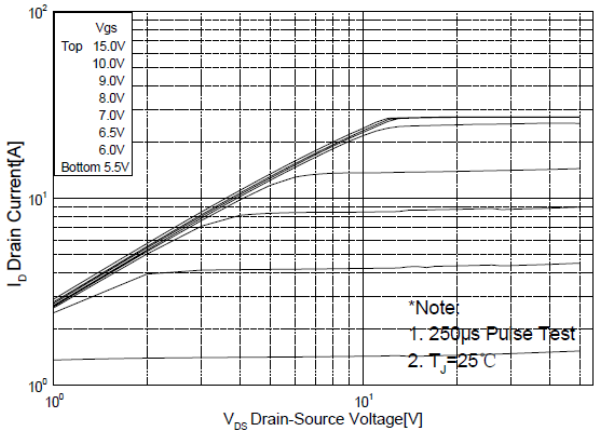


Figure 1. On-Region Characteristics

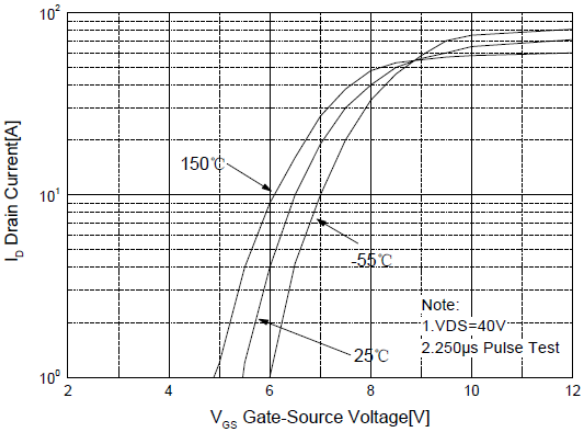


Figure 2. Transfer Characteristics

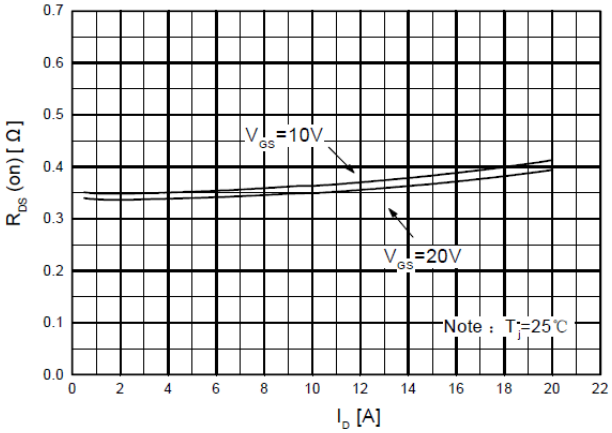


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

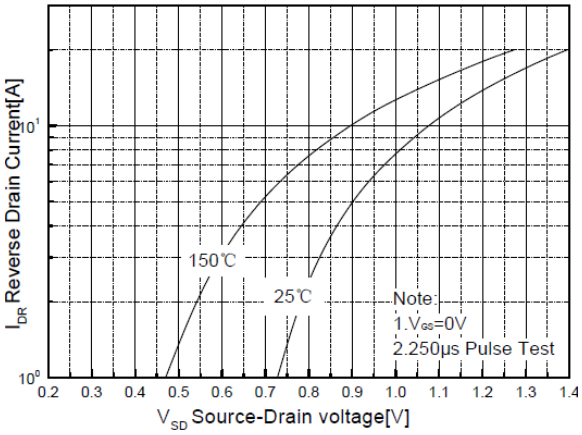


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

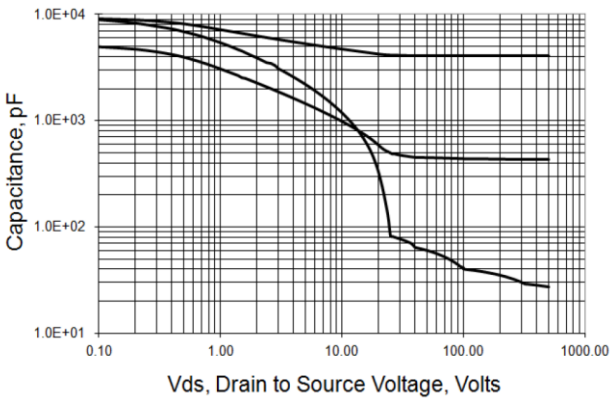


Figure 5. Capacitance Characteristics

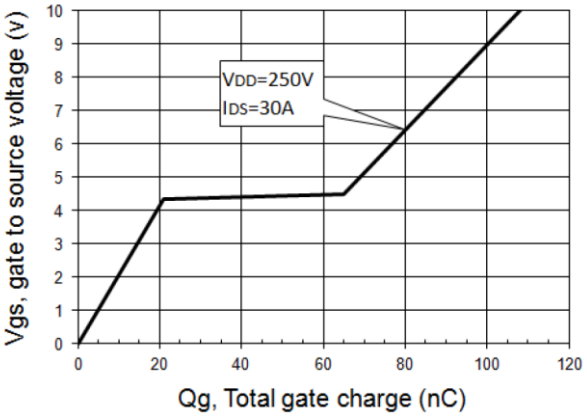


Figure 6. Gate Charge Characteristics

Typical Characteristics

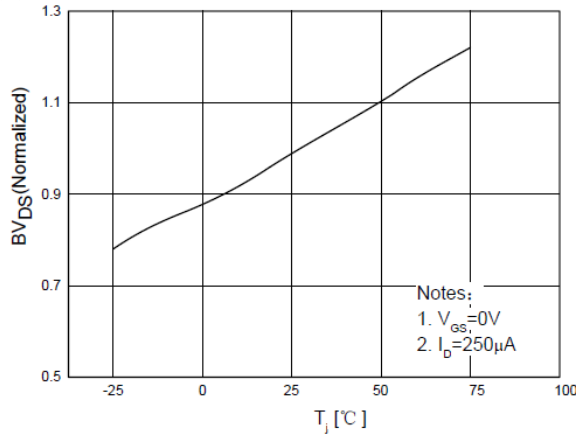


Figure 7. Breakdown Voltage Variation vs Temperature

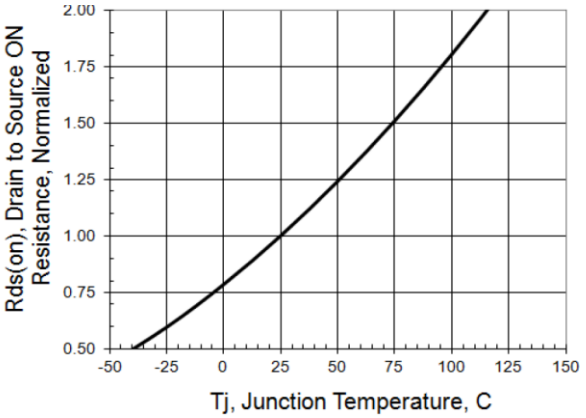


Figure 8. On-Resistance Variation vs Temperature

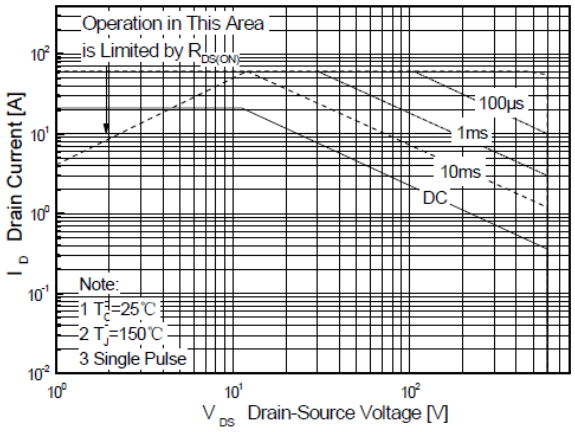


Figure 9-2. Maximum Safe Operating Area for JFAM30N50E

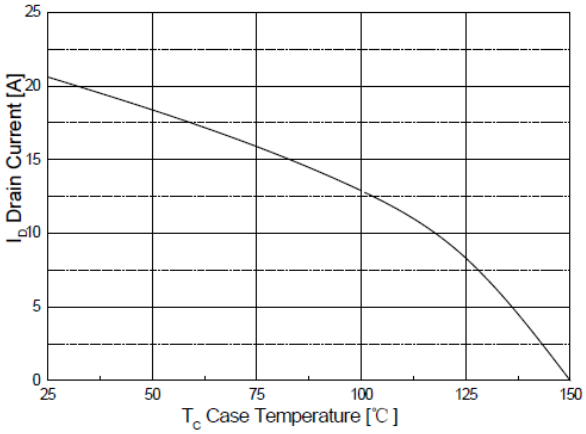


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics

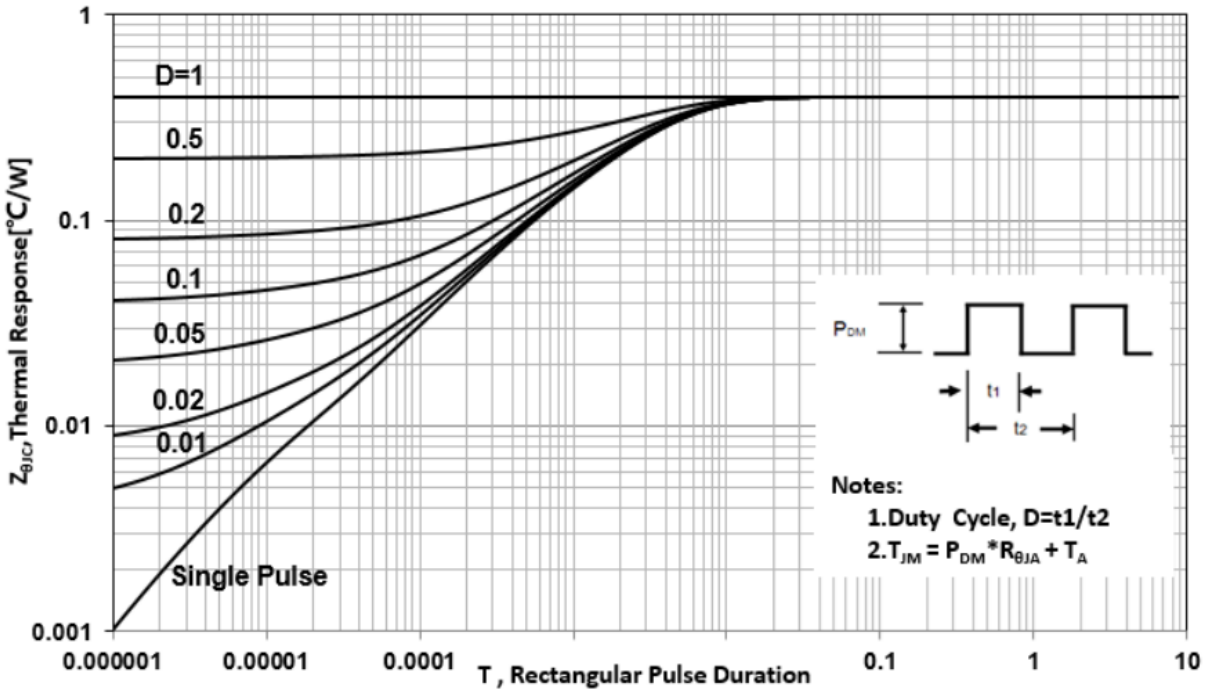
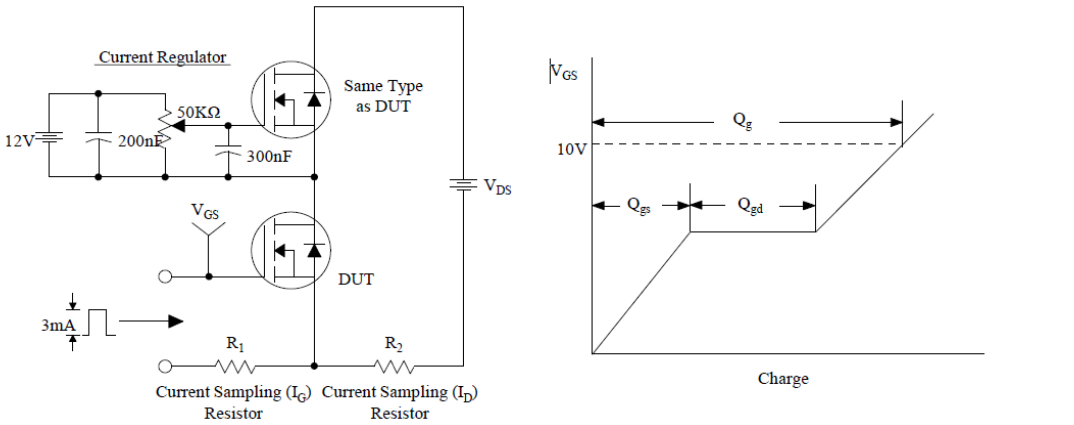
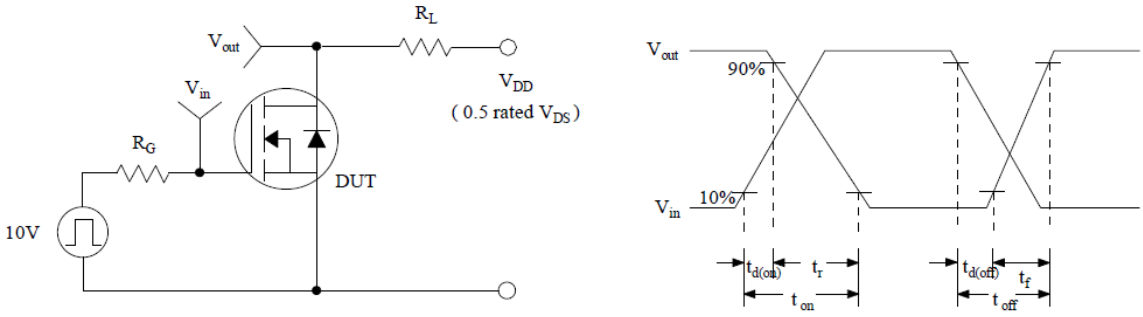


Figure 11-2. Transient Thermal Response Curve for JFAM30N50E

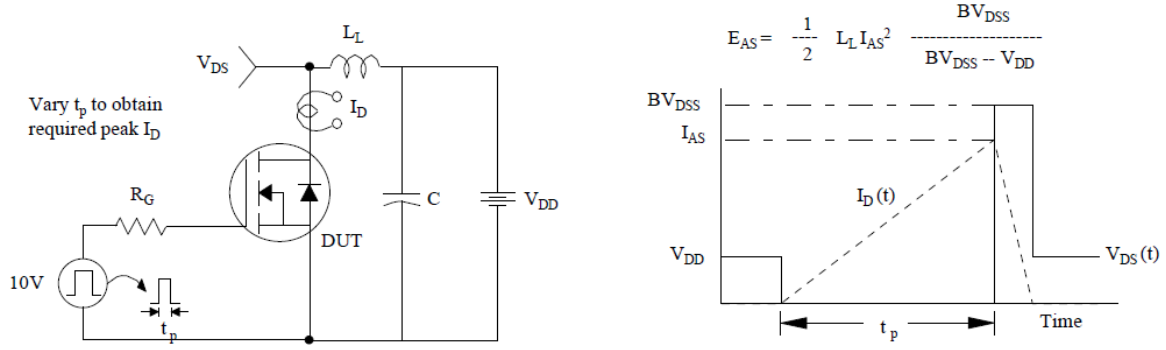
Test Circuit & Waveform



Gate Charge Test Circuit & Waveform

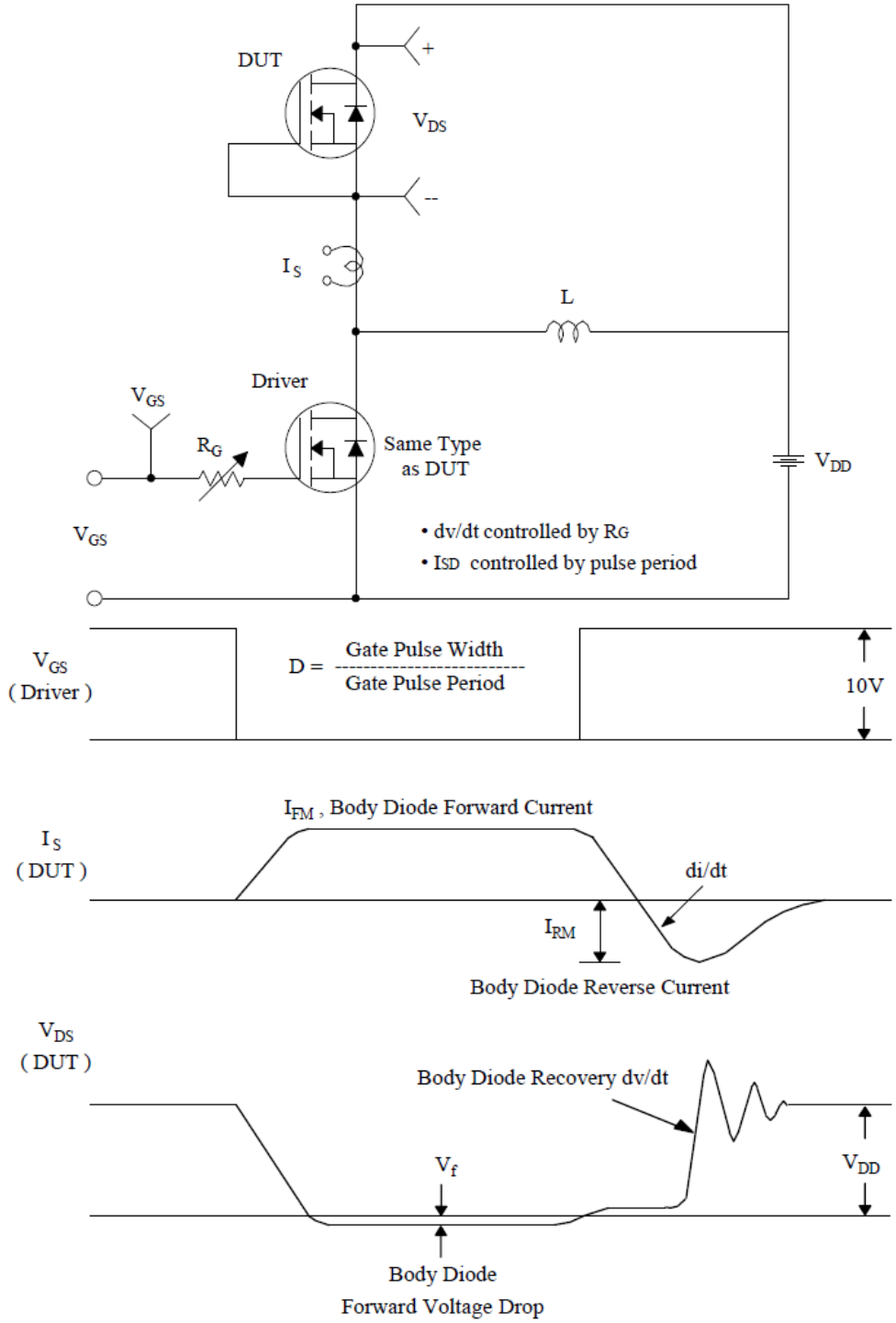


Resistive Switching Test Circuit & Waveforms



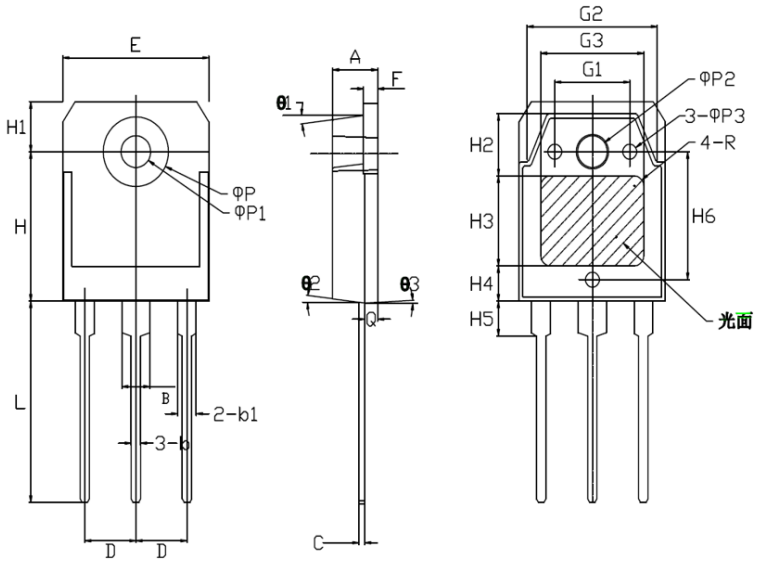
Unclamped Inductive Switching Test Circuit & Waveforms

Test Circuit & Waveform



Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO-3P PACKAGE OUTLINE



符号	单位：mm		
	Min	Nor	Max
*A	4.75	4.80	4.85
*B	2.95	3.00	3.05
*C	0.585	0.600	0.615
*D	5.35	5.45	5.55
*E	15.55	15.60	15.65
*F	1.508	1.500	1.492
G1	7.90	8.00	8.10
G2	13.50	13.60	13.70
G3	10.90	11.00	11.10
b		1.00	
*b1		2.00	
*L	20.00	20.10	20.20
*H	14.80	14.90	15.00
*H1	4.90	5.00	5.10
H2	6.10	6.20	6.30
H3	8.90	9.00	9.10
H4	3.40	3.50	3.60
H5	2.90	3.00	3.10
H6	12.66	12.76	12.86
ΦP		7.00	
*ΦP1		3.20	
*ΦP2		3.50	
ΦP3		1.50	
θ1	6°	7°	8°
θ2	6°	7°	8°
θ3	2°	3°	4°
*Q	1.33	1.38	1.43
R		1.00	

注：1.带*的为检验尺寸。
2.未注公差为0.1mm

Disclaimers

JIAEN Semiconductor Co., Ltd reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to JIAEN's terms and conditions supplied at the time of order acknowledgement.

JIAEN Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing, reliability and quality control are used to the extent JIAEN deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

JIAEN Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using JIAEN's components. To minimize risk, customers must provide adequate design and operating safeguards.

JIAEN Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its parent rights, nor the rights of others. Reproduction of information in JIAEN's datasheets or data books sis permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. JIAEN Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of JIAEN's products with statements different from or beyond the parameters stated by JIAEN Semiconductor Co., Ltd for that product or service voids all express or implied warrantees for the associated JIAEN's product or service and is unfair and deceptive business practice. JIAEN Semiconductor Co., Ltd is not responsible or liable for any such statements.